IMPROVED PERFORMANCE OF DYNAMIC LATCHED COMPARATOR FOR PTL CLOCK GATING CIRCUIT

Dinesh Kumar Ghoghia[1],Rakesh Jain[2],
[1]M.Tech Scholar, Suresh Gyan Vihar University, Jaipur, Rajasthan, India
[2] Assistant Professor, Suresh Gyan Vihar University, Jaipur, Rajasthan, India

ABSTRACT

Comparators are basic building blocks for designing modern mixed signal systems. Speed and resolution are two important factors which are required for high speed applications. This paper presents a design for an on-chip high-speed dynamic latched comparator for high frequency signal digitization. The dynamic latched comparator consists of two cross coupled inverters comprising a total of 9 MOS transistors. The measurement and simulation results show that the dynamic latched comparator with clock gating design has higher speed, low power dissipation and occupying less active area compared to double tail latched and pre-amplifier based clocked comparators. These comparators are used in PTL circuits, so we compared the application of a PTL circuits by using the above specified three comparator designs. The simulation results show that PTL with clock gating circuit dynamic latched comparator has occupied less active area and also having higher speed and lower power dissipation.

***Keywords*— Dynamic Latched Comparator, digitization**

I. INTRODUCTION

The comparator compares the voltages that appear at their inputs and outputs a voltage representing the sign of the net difference between them. The comparator is a circuit that compares an analog signal with another analog signal or reference and outputs a binary signal based on the comparison. If the +, VP, the input of the comparator is at a greater potential than the -, VN, input, the output of the comparator is a logic 1 and vice versa. Comparators are important elements in modern mixed signal systems. Speed and resolution are two important features which are required for high speed applications such as on-chip high frequency signal testing, data links, sense amplifiers and analog-to-digital converters. On-chip testing of high frequency pseudo random binary sequences (PRBS) requires a high speed comparator at the electrical interface stage [1], [2]. A clocked comparator generally consists of two stages. In that first stage is to interface the input signals. The second (regenerative) stage consists of two cross coupled inverters, where each input is connected to the output of the other. In a CMOS based latch, the regenerative stage and its following stages consume low static power since the power ground path is switched off either by a NMOS or PMOS transistor [10]. In many applications comparator speed, power dissipation and number of transistors are more important. If comparator speed is a priority, the regenerative stage could be designed to start its operation from midway between power supply and ground [6], for example, pre-amplifier based clocked comparator [4]. However, the static power consumption is relatively high. If comparator was designed with priority given to power reduction, then number of transistors increases thereby reducing the speed, for example double tail latched comparator[4]. Comparator design largely depends on the target application. However, an input-referred latch offset voltage (hence offset voltage), resulting from the device mismatches such as threshold voltage Vth, current factor β (=μCoxW/L) and parasitic node capacitance and output load capacitance mismatches, limits the accuracy of such comparators [8], [9]. In this paper, we present a design of high-speed and low power dissipating clocked comparator for aircraft applications. This comparator is attractive for the applications where both speed and power consumption is of the highest priority.

In electronics, a comparator is a device that compares two voltages or currents and outputs a digital signal indicating which is larger. It has two analog input terminals V_+ and V_- and one binary digital output V_o. The output is ideally

$$V_o = \begin{cases} 1, & \text{if } V_+ > V_- \\ 0, & \text{if } V_+ < V_- \end{cases}$$

A comparator consists of a specialized high-gain differential amplifier. They are commonly used in devices that measure and digitize analog signals, such as analog-to-digital converters (ADCs), as well as relaxation oscillators.

The differential voltages must stay within the limits specified by the manufacturer. Early integrated comparators, like the LM111 family, and certain high-speed comparators like the LM119 family, require differential voltage ranges substantially lower than the power supply voltages (±15 V vs. 36 V).[1] Rail-to-rail comparators allow any differential voltages within the power supply range. When powered from a bipolar (dual rail) supply,

$$V_{S-} \leq V_+, V_- \leq V_{S+}$$

or, when powered from a uni polar TTL/CMOS power supply:

$$0 \leq V_+, V_- \leq V_{cc}$$

Specific rail-to-rail comparators with p-n-p input transistors, like the LM139 family, allow input potential to drop 0.3 volts below the negative supply rail, but do not allow it to rise above the positive rail.[2] Specific ultra-fast comparators, like the LMH7322, allow input signal to swing below the negative rail and above the positive rail, although by a narrow margin of only 0.2 V.[3] Differential input voltage (the voltage between two inputs) of a modern rail-to-rail comparator is usually limited only by the full swing of power supply.

II. PTL (PASS TRANSISTOR LOGIC)

In electronics, pass transistor logic (PTL) describes several logic families used in the design of integrated circuits. It reduces the count of transistors used to make different logic gates, by eliminating redundant transistors. Transistors are used as switches to pass logic levels between nodes of a circuit, instead of as switches connected directly to supply voltages. This reduces the number of active devices, but has the disadvantage that the difference of the voltage between high and low

logic levels decreases at each stage. Each transistor in series is less saturated at its output than at its input. If several devices are chained in series in a logic path, a conventionally constructed gate may be required to restore the signal voltage to the full value. By contrast, conventional CMOS logic switches transistors so the output connects to one of the power supply rails, so logic voltage levels in a sequential chain do not decrease. Simulation of circuits may be required to ensure adequate performance.

III. CONVENTIONAL COMPARATORS

The circuit and schematic diagrams of the comparator presented in fig 4.1 . This comparator is compared with our design because of its speed and suitability for low supply voltage applications. In the rest of the paper it will be referred to as conventional comparator1.It operates in 2 phases 1)Reset phase 2)Regeneration phase .While the clock is low(reset phase), M7 and M8 transistors are ON. M9 transistor is off. As M7 and M8 transistors are ON Di+ and Di- nodes are pre-charged to Vdd. So M10 and M11 become ON and discharge the output nodes OUT+ and OUT- to ground. While the clock is high (regeneration phase), M9 and M12 transistors are in ON condition. M7 and M8 transistors are in OFF state. So Di nodes starts discharging as M9 is ON. The difference between voltages of Di+ and Di- (ΔVDi) are given to M10 and M11 transistors. As Di nodes starts discharging, M10 and M11 are initially in ON condition and gradually M10 and M11 becomes OFF. Output nodes OUT+ and OUT- starts regenerating when M10 and M11 are unable to ground the outputs. The intermediate stage formed by M10 and Mll passes ΔVDi to the cross-coupled inverters and also provides additional shielding between the input and output, with less kickback noise as a result[8].

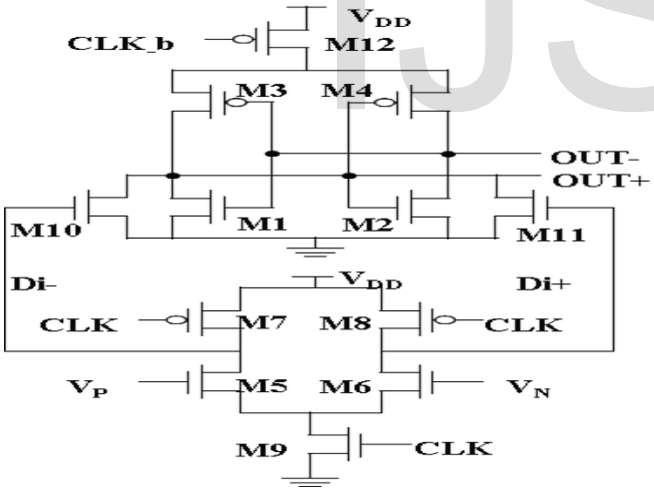

Fig 1 :- Conventional comparator

The first stage is the amplification stage, which consists of the transistors M1–M4 and M9. The second stage is the regenerative stage that is comprised of the transistors M5– M8 and M10. The circuit works in two phases, namely the amplification phase and the regenerative (evaluation) phase. When the clock (CLK) is low (amplification phase), the tail transistor M9 turns ON and M10 turns OFF. When CLK was LOW only amplification stage works here. In addition, the amplification stage is designed to produce its output close to VDD-|Vthp| which can effectively reduce the charging time. In this stage Vp-Vn is amplified and fed to regenerative stage. When the clock (CLK) is high (regeneration phase), M10 turns ON and M9 turns OFF. Only regenerative stage works here. There is a reduction of the delay time in the conventional comparator2 over the conventional comparator1. Since the conventional comparator2 uses an amplification stage, it consumes static power during the amplification period and hence the energy consumption in the conventional comparator2 becomes higher than the conventional comparator1. There is a reduction of the power dissipation in the conventional comparator1 over the conventional comparator2. In order to avoid these drawbacks in conventional comparators, dynamic latched comparator was introduced in the subsequent section.

IV. DYNAMIC LATCHED COMPARATOR

The dynamic latched comparator is composed of two stages . The first stage is the interface stage which consists of all the transistors except two cross coupled inverters. The second stage is the regenerative stage that is comprised of the two cross coupled inverters, where each input is connected to the output of the other. It operates in two phases.1) Interface phase and 2) Regeneration phase. It consists of single nmos tail transistor connected to ground. When clock is low tail transistor is off and depending on Vp and Vn output reaches to VDD or gnd. When clock is high tail transistor is on and both the outputs discharges to ground.

There is reduction of both power and delay in dynamic latched comparator circuit over the two conventional comparators. Conventional comparator1 has less power consumption but low speed because of more transistor count and conventional comparator2 has high speed because of less transistor count but power consumption is more because the conventional comparator2 uses an amplification stage, it consumes static power during the amplification period However, since the conventional comparator2 is to work at high frequency, the energy consumption of the conventional comparator2 becomes comparable to the conventional comparator1. Hence the performance of the conventional comparator2 is limited by the static power dissipation in the evaluation or regeneration phase. The dynamic latched comparator is suitable for both high speed and low power dissipation [12] because of decrease in transistor count which overcomes the problem of two conventional comparators.

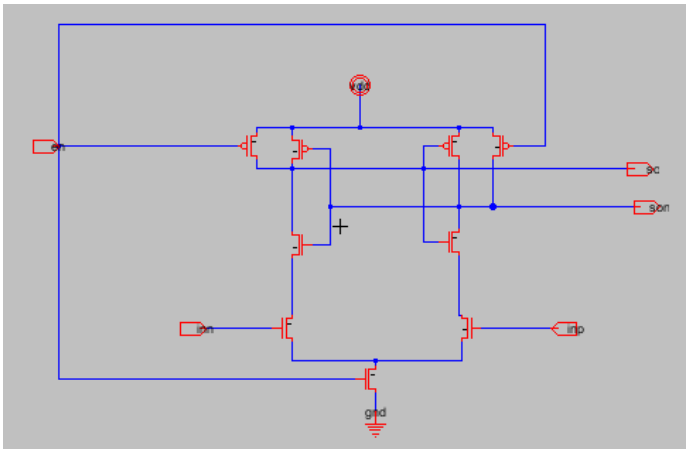

Fig 2:- Schematic of Dynamic latched comparator

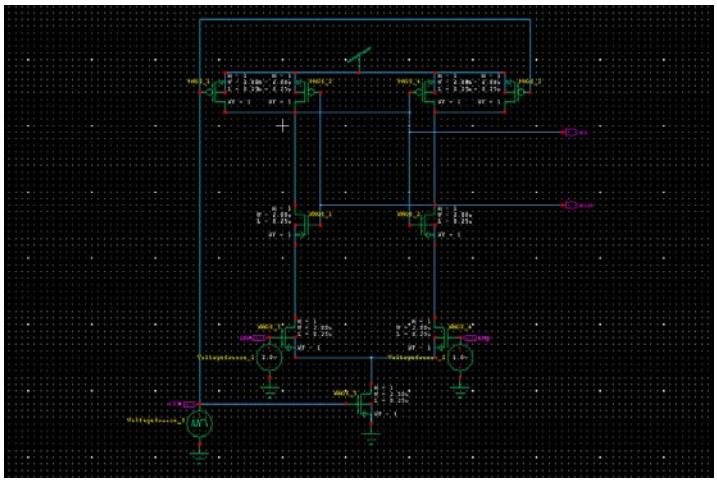

Fig 3 :- dynamic latch comparator

V. DYNAMIC LATCH COMPARATOR WITH PTL

In fig4 sense amplifier was used to recover both voltage swing and performance. If we place either of the conventional comparators or dynamic latched comparator in place of sense amplifier, it is useful to perform two operations. a) To compare the outputs of the stack circuit. As the designed stack circuit performs NOR (or) OR operation, this NOR (or) OR outputs are compared by the clocked comparator.

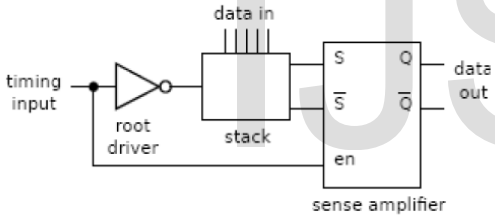

fig 4 :- Architecture of clocked comparator based PTL

b) Combination of both Clocked comparator and stack can also be used as NOR (or) OR circuit. I.e. the output of clocked comparator based PTL (stack) is same as stack circuit (NOR (or) OR circuit). When 'en' (Vin in case of stack circuit) for the comparator was '1', clocked comparator based PTL acts as NOR circuit. When 'en' (Vin in case of stack circuit) was '0' clocked comparator based PTL acts as OR circuit .

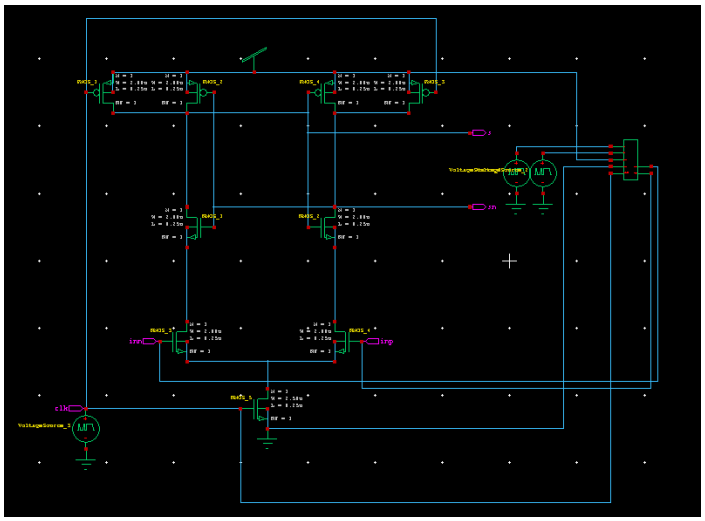

Fig 5 :- dynamic latch comparator by PTL

VI. PROBLEM STATEMENT

Dynamic latch comparator and dynamic latch comparator by PTL circuit is giving high power and delay . When the clock enter in the circuit then circuit will triggered at positive and negative edge of the clock . So when the circuit triggered then it take more power consumption . Circuit will work only at a single edge which can be positive edge and negative edge . dynamic latch comparator is working for single edge so that's why when the circuit triggered then power consumption get more due to triggering. We will give only a single edge at which our circuit is performing .

VII. PROPOSED METHODLOGY

Clock gating is a popular technique used in many synchronous circuits for reducing dynamic power dissipation. Clock gating saves power by adding more logic to a circuit to prune the clock tree. Pruning the clock disables portions of the circuitry so that the flip-flops in them do not have to switch states. Switching states consumes power. When not being switched, the switching power consumption goes to zero, and only leakage currents are incurred.

VIII. DYNAMIC LATCH COMPARATOR BY CLOCK GATING

We are applying clock gating by the NOR Gate . After apply clock gating the circuit will triggered only at a single edge . We apply a NOR gate with clock gating by which only single edge pulses goes in the circuit . In the clock gating we use two nmos with ref. voltage to reduce the logic swing at the output nodes. hence power and time is saved.

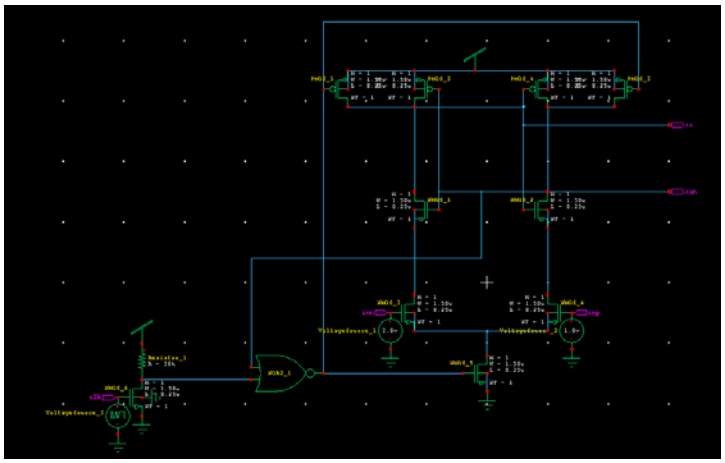

Fig 6:- DTC with clock gating

Same clock gating circuit is apply here .After apply clock gating the circuit able to work on low power consumption . As the extra pulses of the clock reduce then the power consumption of the extra clock will also reduce . By this the circuit get able to reduce the power consumption .

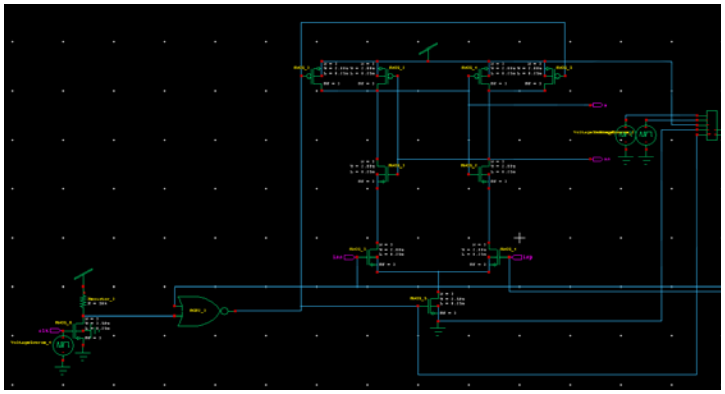

FIg 7 :- DTC by PTL with clock gating

IX. RESULTS

Dynamic latch comparator

The output wave form of the dynamic latch comparator is showing in fig 8. The power consumption of the circuit is 1.818716e-009 W and delay is 1.19ns .

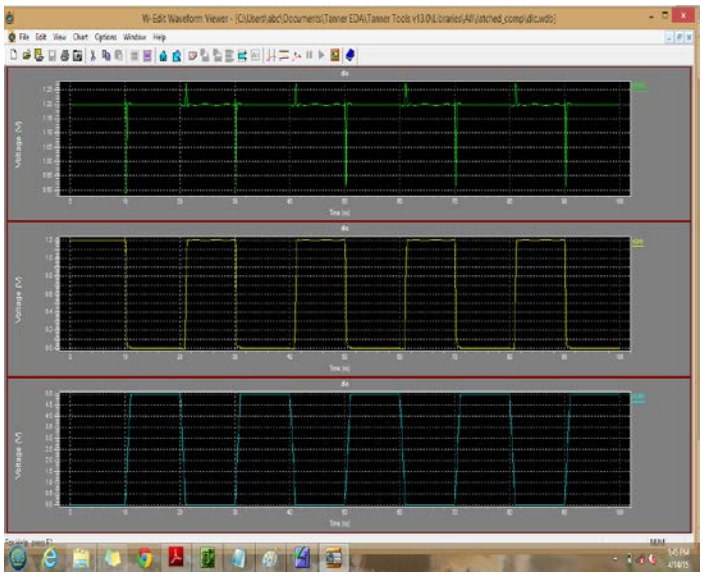

fig 8:- Dynamic latch comparator by Clock gating

The output wave form of the dynamic latch comparator with clock gating is showing in fig 9 . The power consumption of the circuit is 3.554052e-010 W and delay is 1.02ns.

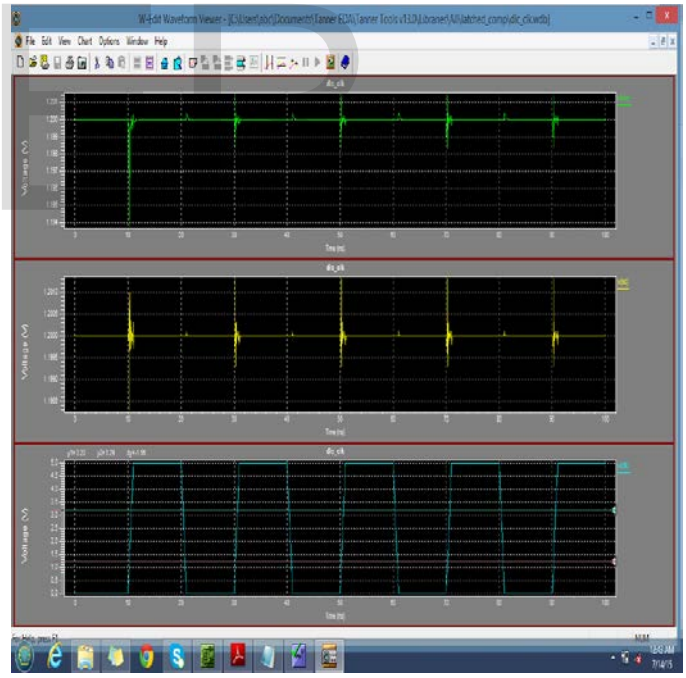

fig 9 :- Dynamic latch comparator by Clock gating

Dynamic Latch Comparator With PTL

The output wave form of the dynamic latch comparator with PTL is showing in fig 10. The power consumption of the circuit is 1.527402e-009 W and delay is 1.02ns.

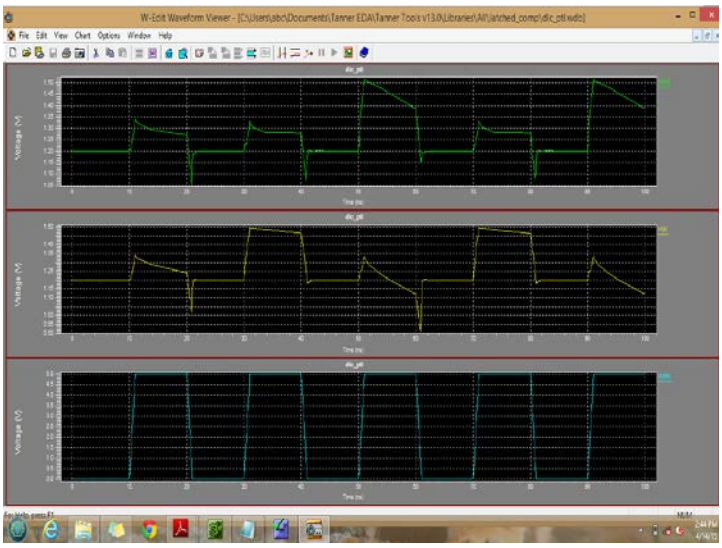

fig 10 :- Dynamic latch comparator with PTL

Dynamic Latch Comparator With PTL By Clock Gating

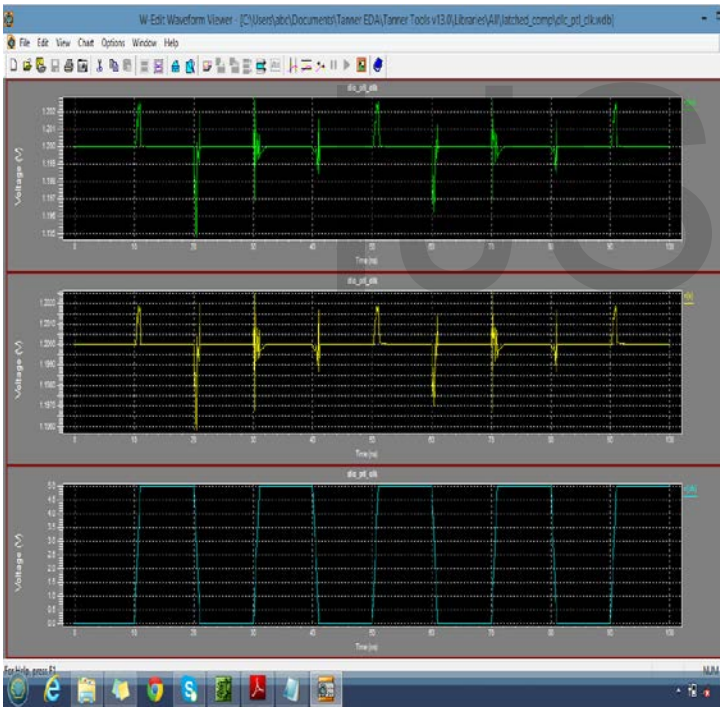

fig 11:- Dynamic latch comparator with PTL by Clock gating

The output wave form of the dynamic latch comparator with PTL by clock gating is showing in fig 11. The power consumption of the circuit is 1.275172e-009 W and delay is 509.80ps .

	Existing		Proposed	
	(DTC)	**(DTC_PTL)**	**DTC_CLK**	**DTC_CLK_PTL**
Power	1.818716 e-009	1.527402 e-009	3.554052 e-010	1.275172 e-009
Delay	1.19ns	1.02ns	1.02ns	509.80ps

Table 1 :- Comparison table

X. CONCLUSION AND FUTURE SCOPE

Dynamic latched comparator was designed that works with high speed and low power consumption when compared to double tail latched comparator (conventional comparator 1) and pre amplifier based latch comparator (conventional comparator 2). For comparison we provide analog input to the comparator and the output will be digital. The simulation results show that the proposed circuit can operate at higher speed with low power dissipation than the other two comparators. Similarly in case of clocked comparator applications such as clocked comparators based PTL, dynamic latched comparator based PTL has less delay time than the other two conventional comparators based PTL. Clocked comparator schematics are implemented in spice and the corresponding layouts are implemented using Tanner tool.

In the future we can improve the results by apply the clock gating in the circuit . By the clock gating we can improve the results because by the clock gating results get improve .Total number of transistor get reduce after apply GDI technique . So by the GDI technique power and delay results get reduce .

REFERENCES

[1] B. Casper, F. O'Mahony, "Clocking analysis, implementation and measurement techniques for high-speed data links: A tutorial," IEEE Trans. Circuits Syst. I, vol. 56, no. 1, pp. 17-39, Jan. 2009.
[2] W T. Beyene et. al. , "Advanced modeling and accurate characterization of a 16 Gb/s memory interface," IEEE Trans. Adv. Package., vol. 32, pp. 306-326, May 2009.
[3] D. Schinkel, et. al., "A Double-tail latch-type voltage sense amplifier with 18ps setup+hold time," in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, San Francisco, CA, Feb. 11-15, 2007, pp. 314-315.
[4] Mohamed Abbas*, Yasuo Furukawa"Clocked Comparator for High- Speed Applications in 65nm Technology,"IEEE Asian Solid-State Circuits Conference November 8-10,2010 / Beijing, China.
[5] LogicLouis Poblete Alarcon and Jan M. Rabaey,"Sense Amplifier-Based Pass Transistor," EECS Department, University of California, Berkeley, Technical Report No. UCB/EECS-2010-173, December 19, 2010.
[6] K. Uyttenhove, M. S. J. Steyaert, "A 1.8-V, 6-bit, 1.3-GHz CMOS flash ADC in 0.25-_m CMOS," *IEEE J. Solid-State Circuits*, vol. 38, no. 7, pp.1115–1122, July 2003.
[7] Jun He, Sanyi Zhan, Degang Chen, and R.L. Geiger, "Analyses of Static and Dynamic Random Offset Voltages in Dynamic Comparators," IEEE Trans. Circuits Syst. I: Reg. Papers, vol. 56, pp. 911-919, May 2009.
[8] Nikoozadeh and B. Murmann, "An Analysis of Latch Comparator Offset Due to Load Capacitor Mismatch," IEEE Trans. Circuits Syst. II: Exp. Briefs, vol. 53, no. 12, pp. 1398-1402, Dec. 2006
[9] Pedro M.Figueiredo, Joao C.Vital, "Kickback Noise Reduction Techniques for CMOS Latched Comparator", IEEE Transactions on Circuits and Systems, vol.53, no.7, pp.541- 545, July 2006.
[10] Meena Panchore, R.S. Gamad, "Low Power High Speed CMOS Comparator Design Using .18µm Technology", International Journal of Electronic Engineering Research, Vol.2, No.1, pp.71-77, 2010.
[11] Heung Jun Jeon, "Low-power high-speed low-offset fully dynamic CMOS latched comparator", Northeastern University, Department of Electrical and Computer Engineering, January 2010.

[12] S. Kale and R. S. Gamad, "Design of a CMOS Comparator for Low Power and High Speed" , Internationl Journal of Electronic Engineering Research, vol. 2, no. 1, pp. 29-34, 2010.
[13] Heungjun Jeon and Yong-Bin Kim, "A Novel Low-Power, Low-Offset and High-Speed CMOS Dynamic Latched Comparator", IEEE, 2010.
[14] ECEN 689 High-Speed Links Circuits and Systems.